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10/783,185	02/20/2004	Yi-Hsien Chuang	PAT-1526	6183

7590  
Raymond Sun  
12420 Woodhall Way  
Tustin, CA 92782

04/19/2007

EXAMINER
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SCHELL, JOSEPH O

ART UNIT	PAPER NUMBER
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2114

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

## Office Action Summary

Application No.

10/783,185

Applicant(s)

CHUANG ET AL.

Examiner

Joseph Schell

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1,3-10,12-19,21-26,28,29,31 and 32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 23-25 is/are allowed.
- 6) ☒ Claim(s) 1,3-10,12-19,21,22,26,28,29,31 and 32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### ***Detailed Action***

Claims 1, 3-10, 12-19, 21-26, 28-29 and 31-32 have been examined.

Claims 1, 3-10, 12-19, 21-22, 26, 28-29 and 31-32 have been rejected.

Claims 23-25 are allowable.

### ***Response to Arguments***

1. Applicant's arguments filed January 24, 2007 have been fully considered but they are not persuasive. Specifically, Applicant argues that Boyce ('258) does not teach or suggest a debugger service routine that parses requests that are stored and issued by a debugger RAM. The Examiner respectfully disagrees. As stated by Boyce ('258) in column 3, lines 39-54, the user designates an instruction, the mainframe converts the user instruction to appropriate code, and the command is input into monitor memory, and the target processor executes its NOOP loop and executes the instruction. The parsing occurs when the user input is converted to target-specific instructions.

The rejections of claims 5 and 14 under 35 U.S.C. 112, regarding the indefiniteness of "free-run", "step-into", and "stop test" are withdrawn.

### ***Allowable Subject Matter***

2. Claims 29 and 31-32 contain allowable subject matter. The following is a statement of reasons for the indication of allowable subject matter: Within claims 29 and 32 the examiner deems the novel limitation to be that the parsing of user input is performed by a routine stored on the target microcontroller.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 3-10, 12-19, 21-22, 26, 28-29 and 31-32 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Specifically, independent claims 1, 10, 19, 26, 29 and 32 contain (in the second to last paragraph of all claims except 29 and 32, wherein the limitation is about 2/3's of the way through the claim) the limitation "the debugger RAM storing and issuing requests." This limitation, of the debugger RAM *issuing* requests, is not supported by the specification. The examiner is assuming the debugger RAM instead passively stores requests such that they are available for retrieval.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 3-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Boyce ('258).
5. As per claim 1, Boyce ('258) discloses an apparatus for debugging an electronic system, said electronic system including a target microcontroller (MCU) and at least one ROM connected together (column 2 lines 43-48), comprising:
  - debugger unit which debugs said target MCU (column 1 lines 49-52);
  - a ROM/RAM emulator/debugger unit, connected to said target MCU and said debugger unit, for emulating said ROM (column 1 lines 49-52), and including:
    - a ROM/RAM emulation memory, connected to said emulator/debugger unit, for storing user program codes downloaded from said debugger unit (column 2 lines 67-68 and column 3 lines 15-20);
    - an emulator/debugger microcontroller (MCU), coupled to said emulator/debugger unit, for communicating with, and performing requests from, said debugger unit and said target MCU (column 1 lines 57-61 and 2 lines 43-48, while a microcontroller is not explicitly stated, it is required to perform the stated functions);

a bus mapping unit, coupled to said emulator/debugger MCU (column 2 line 67 through column 3 line 2);

a debugger RAM unit, coupled to said emulator/debugger MCU (as shown in Figure 3 part of the ROM emulator's memory is dedicated to monitor code, see also column 3 lines 10-12), the debugger RAM unit storing and issuing requests (column 3 lines 45-49); and

a debugger service routine ("debugger SR") downloaded from said debugger unit into said ROM/RAM emulation memory (column 3 lines 456-48) with said user program codes from said debugger unit (column 1 lines 49-63, user-created debug functions are stored on the ROM, in addition to the command instruction dynamically added to cause the processor to jump to the debug code (column 3 lines 41-43)), the debugger SR parsing the requests issued by the debugger RAM unit (column 1 lines 57-61 and column 3 lines 49-52).

6. As per claim 3, Boyce (258) discloses the apparatus of claim 1, further comprising a communication buffer implemented in said emulation memory, said communication buffer being disposed to store status, request and data by said target MCU and by said emulator/debugger MCU (column 3 lines 49-54, execution results are returned to the debugger, and execution status is conveyed the execution results. Also see column 2 lines 45-47, command fragments of debug routines are passed through the communications buffer).

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7. As per claim 4, Boyce ('258) discloses the apparatus of claim 3, wherein said target MCU executes said debugger SR to:

copy a "loop to itself" instruction to said debugger RAM unit and then jump to said copied instruction to release access of said ROM/RAM emulation memory (column 3 lines 13-15 and 20-25);

inform said debugger unit upon executing a software breakpoint or upon completing requests from said emulator/debugger MCU (column 3 lines 49-54, the results are shown on the host debugger's display); and

parse requests from said emulator/debugger MCU to perform actions, wherein said requests are stored in one of said emulator/debugger RAM unit and said communication buffer (column 2 lines 45-47).

8. As per claim 5, Boyce ('258) discloses the apparatus of claim 1, wherein said debugger unit is disposed to:

download and upload user program codes to and from the emulator/debugger MCU (column 3 lines 15-20);

set, delete, enable and disable breakpoints (column 3 lines 39-42);

writes codes to the ROM/RAM emulation memory (column 3 lines 39-42);

show and modify registers and memory (column 3 lines 39-42); and

perform free-run, step-into, step-out and stop test steps (column 3 lines 39-42, the removal or placement of breakpoints controls the flow of a test routine).

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9. As per claim 6, Boyce ('258) discloses the apparatus of claim 5, wherein said debugger RAM unit is disposed to:

store data for said target MCU to modify its debugging state and data (column 3 lines 39-42, modification of breakpoints changes the debug state and data);

store a request for said target MCU (column 3 lines 48-49);

store debugging status and data of said target MCU for uploading to said debugger unit after said target MCU has finished said request (column 3 lines 49-54);

and

provide program spaces for said target MCU to execute programs in order to release access to said ROM/RAM emulation memory (column 3 lines 13-15).

10. As per claim 7, Boyce ('258) discloses the apparatus of claim 1, wherein said bus mapping unit maps said debugger RAM unit to a specified address space, which is different from said ROM/RAM emulation memory, to form a continuous and linear addressing space (column 3 lines 10-13, and as shown by Figure 3 with the separate memory addresses for user code and monitor instructions).

11. As per claim 8, Boyce ('258) discloses the apparatus of claim 3, wherein said emulator/debugger MCU passes debugging requests to said target MCU by one of:

a) said emulator/debugger MCU storing requests in said debugger RAM unit (column 1 lines 49-57);



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said emulator/debugger MCU informing said target MCU to perform said requests

(column 1 lines 54-56, the user initiates an interrupt);

said target MCU executing programs in said ROM/RAM emulation memory (column 1 lines 56-57); and

b) said emulator/debugger MCU informing said target MCU to perform said requests (column 1 lines 54-56);

said emulator/debugger MCU informing said target MCU to copy a "loop to itself" instruction to said debugger RAM unit (column 3 lines 20-22) ;

said target MCU jumping to said copied instruction to release access to said ROM/RAM emulation memory (column 3 lines 33-41); and

upon release by said target MCU, said emulator/debugger MCU storing requests in said communication buffer and informing said target MCU to perform said requests (column 3 lines 39-49).

12. As per claim 9, Boyce ('258) discloses the apparatus of claim 8; wherein said emulator/debugger MCU returns data and status to said debugger unit by way of one of the following:

a) after said target MCU has executed a software breakpoint instruction, after being informed by said target MCU, said emulator/debugger MCU uploads the content of one of said debugger RAM unit or communication buffer to said debugger unit (column 3 lines 32-49 and column 3 lines 55-57); or

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b) after said target MCU has finished a request by said debugger unit, after being informed by said target MCU, said emulator/debugger MCU uploads the content of one of said debugger RAM unit and communication buffer to said debugger unit.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 10, 12-19, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyce ('258) in view of Autrey (US Patent 5,774,695).
14. As per claim 10, Boyce ('258) discloses an apparatus for debugging an electronic system, comprising:
  - a target board that includes a target MCU that has a ROM (column 2 lines 21-24);
  - a debugger unit for debugging said target MCU (column 2 lines 43-48, the mainframe);
  - a ROM/RAM emulator board, connected to said debugger unit, for emulating said ROM of said target MCU, said emulator board including a ROM/RAM emulation memory and an emulator MCU, said ROM/RAM emulation memory being disposed to

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store user program codes downloaded from said debugger unit, and said emulator MCU being disposed to read and write data from and to said ROM/RAM emulation memory; and

a debugger service routine ("debugger SR") downloaded from said debugger unit into said ROM/RAM emulation memory (column 3 lines 456-48) with said user program codes from said debugger unit (column 1 lines 49-63, user-created debug functions are stored on the ROM, in addition to the command instruction dynamically added to cause the processor to jump to the debug code (column 3 lines 41-43)), the debugger SR parsing the requests issued by the debugger RAM (column 1 lines 57-61 and column 3 lines 49-52).

Boyce ('258) anticipates a system wherein the emulation board is directly connected to a host mainframe (as shown in Figure 2). Boyce ('258) does not expressly disclose the system comprising a debugger board including a debugger MCU for communicating with said debugger unit and with said target MCU, and for performing requests from said debugger unit and said target MCU, said debugger board further including a bus mapping unit, and a debugger RAM.

Autry ('695) teaches a system that uses a network adaptor to interface a debugging host with an emulator (see abstract). This adaptor necessarily includes a bus mapping unit (column 3 lines 25-28, the system converts network transmissions to emulator

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instructions) and RAM (column 8 lines 25-29, the communications manager performs fairly complicated protocol detection and selection algorithms).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the emulation system disclosed by Boyce ('258) such that it includes the network adaptor communication device, as disclosed by Autrey ('695) between the emulator board at the host mainframe. This modification would have been obvious because the use of physical connection hardware increases setup time (Autrey ('695) column 2 lines 29-32) and limits the tester to a physical location near the system under test (Autry ('695) column 2 lines 35-38).

15. As per claims 12-18, these claims recite limitations found within claims 3-9, respectively. Accordingly, claims 12-18 are rejected under Boyce ('258) in view of Autrey ('695) on the same grounds as cited with the respective 102(b) rejections of claims 3-9, above.

16. As per claim 19, this claim recites limitations found within claim 10, with the additional limitation of a the system comprising a debugger MCU, for communicating with said debugger unit and with said target MCU, and for performing request from said debugger unit and said target MCU.

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In the system disclosed by Boyce ('258) a debug tool is used in conjunction with a mainframe computer with which a user performs debugging (column 1 lines 47-49).

The mainframe translates a user's instructions into microprocessor-specific code (column 1 lines 49-52) and this requires a control unit.

17. As per claim 21, this claims recite limitations found within claim 3. Claim 21 is rejected under Boyce ('258) in view of Autrey ('695) on the same grounds as cited with the 102(b) rejections of claims 3, above.

18. As per claim 22, Boyce ('258) in view of Autrey ('695) discloses the apparatus of claim 19, further including a target/debugger board, connected to said debugger RAM board, that includes said target MCU and said debugger MCU.

19. Claims 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyce ('258) in view of Winegarten (US Patent 6,691,266).

20. As per claim 26, Boyce ('258) discloses an apparatus for debugging an electronic system, said electronic system including a micro-controller ("target MCU") and at least one ROM connected together (column 2 lines 43-48), comprising:

- a debugger unit for debugging said target MCU (column 1 lines 49-52);
- a ROM/RAM emulator board, connected to said debugger unit (column 1 lines 49-52), said emulator board being disposed to emulate said ROM of said target MCU

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(column 1 lines 49-52), said emulator board including a ROM/RAM emulation memory and an emulator MCU (column 1 lines 57-61 and column 2 lines 43-48, while a microcontroller is not explicitly stated, it is required to perform the stated functions), said emulation memory being disposed to store user program codes downloaded from said debugger unit (column 2 lines 43-48), said emulator MCU being disposed to read and write data from and to said ROM/RAM emulation memory (column 2 lines 43-48); and a target/debugger board, connected to said emulator board and to said debugger unit, said target/debugger board including said target MCU (column 1 lines 47-52, while not physically connected, the mainframe is functionally connected to the target through the emulator); and

a debugger service routine ("debugger SR") downloaded from said debugger unit into said ROM/RAM emulation memory (column 3 lines 456-48) with said user program codes from said debugger unit (column 1 lines 49-63, user-created debug functions are stored on the ROM, in addition to the command instruction dynamically added to cause the processor to jump to the debug code (column 3 lines 41-43)), the debugger SR parsing the requests issued by the debugger RAM unit (column 1 lines 57-61 and column 3 lines 49-52).

Boyce ('258) does not explicitly disclose the system including a debugger MCU, implemented with said target MCU, for communicating with said debugger unit and said target MCU, and for performing requests from said debugger unit and said target MCU,

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said debugger MCU including an embedded RAM; and wherein the target/debugger board includes said debugger MCU and an embedded RAM.

Winegarden ('266) teaches an integrated circuit with an internal debugging unit that communicates with an external controller and an internal controller (the FPGA). The integrated circuit also contains memory (all as shown in figure 6).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the emulator system disclosed by Boyce ('258) such that the target chip includes an internal debugging unit that communicates with an external controller and an internal controller as shown by Winegarden ('266). This modification would have been obvious because the bus freezing causable by the debugger unit allows for increased hardware debugging flexibility (Winegarden ('266) column 6 lines 24-27).

21. As per claim 28, Boyce ('258) in view of Winegarden ('266) discloses the apparatus of claim 26, further comprising a communication buffer implemented in said emulation memory, said communication buffer being disposed to store status, request and data by said target MCU and by said debugger MCU (Boyce ('258) column 3 lines 49-54, execution results are returned to the debugger, and execution status is conveyed the execution results. Also see column 2 lines 45-47, command fragments of debug routines are passed through the communications buffer).

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS



SCOTT BADERMAN  
SUPERVISORY PATENT EXAMINER